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IMPLEMENTATION OF DIGITAL DOWN CONVERTER AND PULSE COMPRESSION IN DIGITAL RECEIVER

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ABSTRACT

This paper focuses on Digital Down Converter (DDC) and Pulse compression design and implementation for a Digital receiver. The use of multi-processor system-on-chip (SoC) technologies has enabled the replacement of analog hardware modules with software-driven heterogeneous complex blocks in electronic communication systems. Wideband signals are used for confidential communication. The received signal is an RF signal using linear frequency modulation (LFM), which has a high data rate, and intermediate frequency (IF), which goes through frequency selection to change from an unstable IF signal to a stable IF signal. The input of the ADC is the received signal, and the output is given to the DDC. A digital down converter pulls the data necessary for the digital pulse compression technique from the band- limited high sampling rate modulated signal.Pulse compression, which is often used in RADAR, allows for peak power constraints to be overcome as well as improved range resolution and tolerance to mutual interference. The proposed design includes a wide band DDC with a decimation factor of 8, realized using Verilog HDL with Vivado 2018.2. and MATLAB.

Keywords:
Digital down converter, Pulse compression, Linear Frequency modulation, Fast Fourier Transform, (LFM) Linear Frequency Modulation.

INTRODUCTION

"Narendra N, Degala Sri Lakshmi, Mohan Kumar V", Design of DDC and Signal Detection Techniques for SDR", 2019. In this paper they described as Software Defined Radio with high- end multi-processor SOC technology leads to exchange of Hardware Blocks with Software Driven Flexible Heterogenous complex blocks

using VHDL programming in FPGA. Here DDC design is processed for Downsampling with a selected Decimating factor. The input data rate from Analogue to Digital Converter to Digital Down Converter is 100MHz, whereas the output sampling rate is 50MHz, with decimation factors of 2 and 4 obtaining 25MHz.

"H. A. Said. A. El-Kouny, A. E. El-Henawaey", "Design and Realization of Digital Pulse Compression based on LFM Waveforms using FPGA", 2013. In this paper they described The proposed design is a one-chip solution to produceand receive pulse compression using VHDL. The FPGA offers flexibility, assumes reconfiguration in milliseconds.

"Fan Wang, Huotao Gao, Lin Zhou, Qingchen Zhou, Jie Shi, Yuxiang Sun", "Design and FPGA implementation of digital pulse compression for HF radar based on orthogonal transformation", IEICE Electronics Express, Vol.8, P1736-1742, October-25-2011. The received signal is connected with a Chirp-UWB template waveform, and the integral period is calculated using the UWB sweep function and bands. By altering the integral period, arbitrary band signals may be identified. The sweep function increases detection performance, and measures such as Miss Detection Error Rate and False Alarm Rate are used to assess the technique's usefulness.

"Kohei Ohno, Makoto Itami, Tetsushi Ikegami", "An Interfering Signal Detection Technique Using an Ultra-Wideband Chirp Template Waveform", Wireless communications, Volume 62, Springer, (617-632), February-2012. This paper introduces a Pulse Compression method for HF radar. The focus is performing the de-chirp operation on an FPGA chip through modified orthogonal transformation. This approach

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enables an all- digital receiver platform that directly samples the RF received signal. Compared to traditional

analog or IF receivers, it offers a simpler hardware structure resembling a "soft" radar mode. The design is validated through system closed-loop tests, demonstrating its correctness and suitability for practical applications.

OBJECTIVES AND MOTIVATION

Since Ancient times, communication systems haverelied on hardware-based methodologies. AsModern trends are moving from hardware to digital methodologies. This approach of SoftwareDigital Receiver is to have a direct interaction between ADC/DAC and antenna. In Software Digital Receivers, the DUC is used in the transmitter, while the DDC is used in the receiver. The DUC up-translates a complex-conjugate digital input signal to a digital intermediate frequency (IF), which is then converted to analog IF output using a digital-to-analog converter (DAC). DDC simplifies SDR design and provides flexibility in programming IF bandwidth. This paper focuses on the DDC component. Its main objective is to detect signals as a wideband using Fast Fourier Transform (FFT) techniques. Whereas analog methodologies, FFT has simultaneous processing and detection of all signals. The noise floor estimation is automatically detected within the spectrum. In Digital DownConverter, FFT blocks are designed to achieve a bandwidth of 40 MHz Due to high bandwidthdemand, FPGA-based hardware is implemented. The design is also flexible, allowing for Verilog code porting to different FPGA or FPGA-based MP-SoC (Multiprocessor System-on-Chip) hardware. Finally, the design is based on the programming of IF, LO, and Bandwidth by using Verilog code.

PROPOSED METHODOLOGYBLOCK DIAGRAM

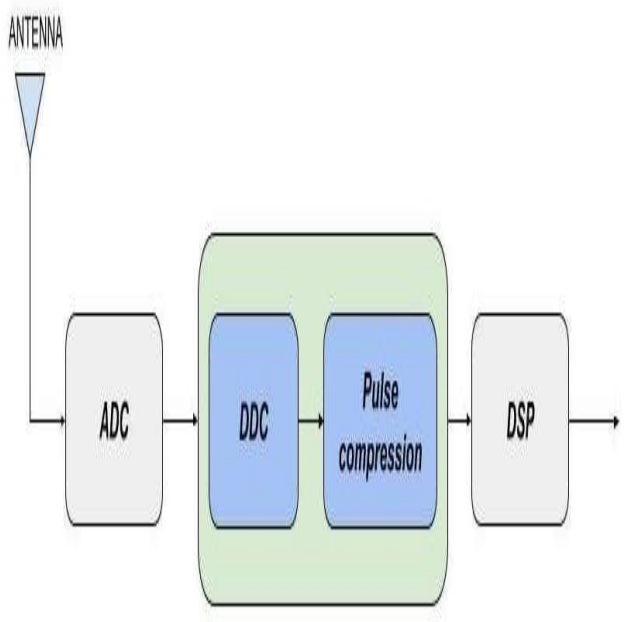

Figure 1 Digital Receiver block Diagram

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DDC

Digital Down Conversion (DDC), is a method thataccesses a high sampling rate data, limits its frequency range, and shifts the baseband to a low frequency while preserving the information. Using a mixer, it transforms an electronic signal on a sinewave input filter (IF) to a complex signal to a zero(0) frequency centered. Additionally, DDCusually reduces the sample rate through multiple stages of decimation filters. This lower-rate signalis easier to process on a slower processor. The main benefit of DDC is a baseband with specifiedBW. The DDC consists of:

A. Numerically Controlled Oscillator
B. Mixer or Multiplier
C. Cascaded Integrator Comb filter
D. Compensating FIR filter.

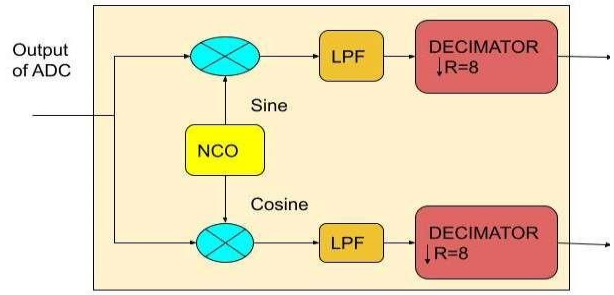

Figure 2 Block diagram of DDC

NCO

The Numerically Controlled Oscillator is adigital synthesizer that provides in-phase and quadrature waveforms The NCO employs the memory look-up table approach, in which the amplitude values of the inphase and quadrature signals are digitally recorded in a read-only memory (ROM). To prevent alias and ensure accurate signal reconstruction, the Nyquist- Shannon theorem states that a minimum of two samples per cycle is needed. The phase accumulator value increment is

$$\theta=F_{clk}/2^{N} \qquad (1)$$

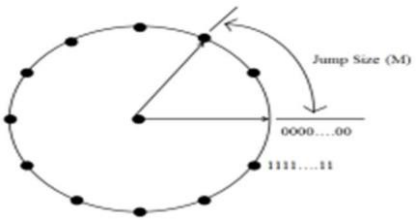

Figure 3 Phase Wheel

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Phase accumulator

The "Phase Accumulator" is the key component ofNCO. It gets updated during each clock cycle. When it is triggered, the phase accumulator adds the phase increased (Δf) to its current contents. The tuning word determines the step size betweenupdates of the reference clock. It specifies thenumber of points to skip on the phase wheel, whichfunctions similarly to a angular rotation around thephase wheel. Each phase wheel points represents asample of a whole sine wave. The phase accumulator (PA) replaces an address counter andadds the tuning word to the stored number in the phase register each time it gets a clock pulse.

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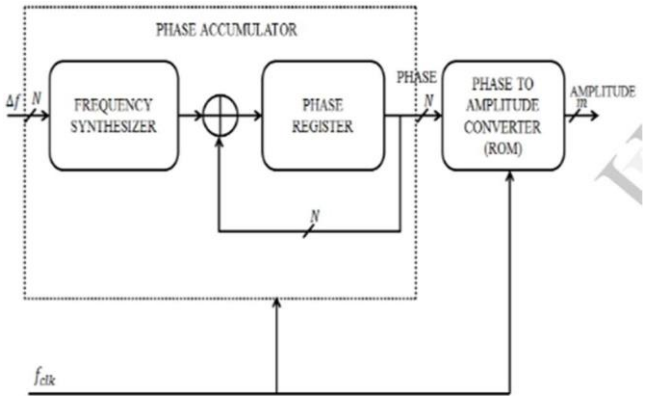

Figure 4 PA

$$f_{out} = \frac{(\Delta f * f_{clk})}{2^N}$$

Where

Δf = Frequency Tuning Word

$fout$ = output frequency

N = number of bits to represent FTW

$fclk$ = Clock frequency

Output of the PA (in degrees) is obtained byusing the below formula,

$$Phase\ Accumulator\ Output\ PA = \frac{(n * \Delta f * 360°)}{2^N}$$

PAC:

The Look-Up Table (LUT), commonly known as the Phase to Amplitude Converter (PAC), is aquadrature and in-phase LUT. It obtains a waveform LUT by using the N-bit output of the

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word from PA as an address. The LUT returns the sine amplitude at that phase point. The output value at the PAC is,

$$PAC\ output\ x(n) = sin(PA)$$

If "n" indicates the no. of bits used to represent the truncated phase, a Sine/Cosine can be implemented as Read-Only Memory (ROM) that stores 2^N samples. These samples represent the waveform in the sample domain and are created based on the phase values received from the Phase Accumulator (PA). Essentially, the LUT converts the phase values from PA into corresponding amplitude. The digital phase values also serve as the memory location for retrieving the LUT's associated amplitude.

To convert an Intermediate Frequency (IF) to a baseband signal, a mixer is employed. The mixer accomplishes the multiplication of the baseband with a computational sinusoidal signal, specifically cos(wt) - j sin(wt) = e^(-jwt). As a result of the multiplication, the mixer produces two output signals that are 90 degrees out of phase with each other.

Mixer

Aliasing can occur at the mixer step due to the mixing of multiple frequencies. These aliasing must be removed in following phases utilising filtering techniques. Filtering removes undesirable frequencies and artefacts, preserving the intended baseband signal while suppressing undesired aliasing.

i. I-Phase signal

ii. Q-Phase signal

This works on the following principle:

Frequency A * Frequency B = Frequency (A-B) +Frequency(A+B)

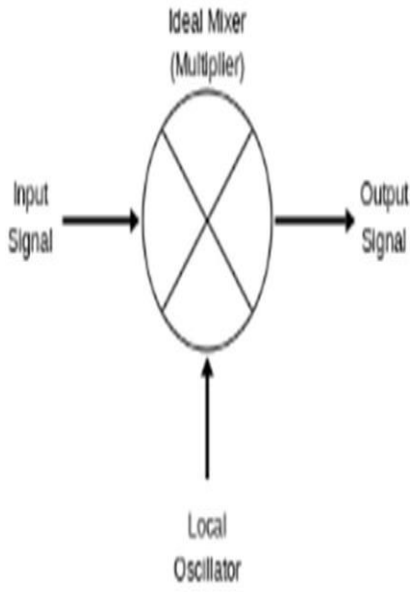

Figure 5 Block Diagram of Ideal Mixer

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Low pass Filter (CIC filter)

Cascaded Integrated Comb (CIC) filters are commonly used in digital systems to achieve significant sample rate changes. These filters are rely on adders, subtractors, and registers. They are especially helpful in applications where the sample rate of the system is significantly greater than the bandwidth of the signal, resulting in a huge surplus sampling rate. A sequence of digital integrators are followed by an equal number of digital comb filters in the CIC filter structure. A digital switch is positioned between the integrators and the combs to lower the sampling frequency of the comb filter signals in comparison to the integrator signals. This cascade of integrators and combs helps in achieving the desired sample rate reduction while maintaining the necessary filtering characteristics. The integrators perform a cumulative summation, providing low-pass filtering, while the combs act as differentiators. This combination allows for effective sample rate conversion and filtering without the need for complex multiplication operations.

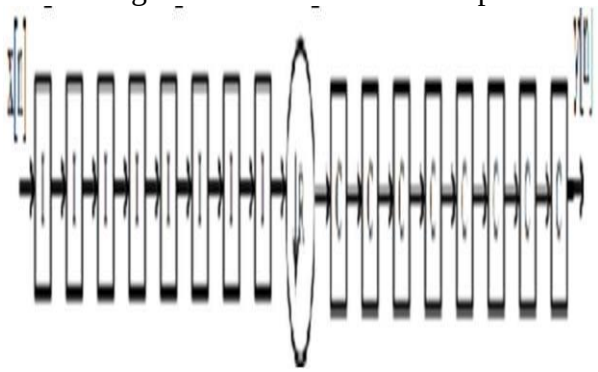

Figure 6 CIC filter

Decimator (CFIR filter)

CIC filter output exhibits a sinc shape, which may not be ideal for many applications due to passband drop and undesired filter characteristics. To overcome these limitations, a "clean-up filter" added to CIC filter output. The cleanup filter serves two purposes. First, it corrects the passband drop, ensuring a more flat response of the desired frequency range. Second, it allows for customization of the cutoff frequency and filter shape according to the specific requirements of the application. Typically, the cleanup filter also includes a decimation stage, reducing the output sample rate by a factor of 2\4. This helps minimize the number of output samples, making the signal processing more efficient and manageable. By applying the cleanup filter after the CIC filter, the output signal can be improved in terms of its frequency response and overall filter characteristics, making it more suitable for various applications.

$$y(n) = b_0x(n) + b_1x(n-1) + \ldots\ldots\ldots + b_Px(n-P)$$

The magnitude response of CFIR is shown in the following equation.

$$H(f) = \left|MR\frac{\sin\pi f}{\sin(\pi RMf)}\right|^N \approx \left|\frac{\pi MRf}{\sin(\pi RMf)}\right|^N = |\sin c^{-1}(MRf)|^N$$

Decimator (PFIR filter)

In the final stage of the signal processing, an equiripple filter is used to provide additional filtering and using decimation factor of 8. This filter, known as the Post-FIR (PFIR), serves as the last stage of down-conversion. The PFIR filter shares similar characteristics with the previously mentioned CFIR (Clean-up FIR) filter, but with a different number of filter coefficients. In this case, the PFIR filter utilizes 41 filter coefficients to achieve the desired filtering performance. The output obtained represents the final DDC output of the system. Overall, the PFIR filter plays a crucial role in fine-tuning the frequency response and achieving the desired signal characteristics before the final output is obtained.

Pulse compression

Pulse compression is a method used in radar signal processing to detect echoes by compressing the received signal in time. It can be accomplished through a correlation operation using a matched filter. In the described model, four FIR filters with Rand I parts are used to process the input signal. The signal reference,

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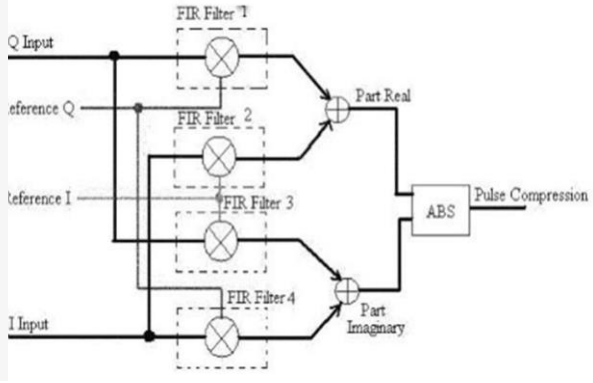
representing the transmitted signal, is also presented in R and I parts. The R and I parts of the pulse compression are obtained by adding output of specific FIR filters. The resulting complex signal is then processed using the ABS CORDIC algorithm to calculate its absolute value. This approach helps overcome issues like zero frequency andinterference, enabling effective tracking



$$R_{xx}(m) = \sum_{n=-\infty}^{\infty} x(n)h(m-n)$$

$$R_{xx}(m) = x(n) * x^*(-n)$$

$$R_{xx}(m) = IFFT[FFT\{x(n)\} \times FFT\{x^*(-n)\}]$$

Figure 7 Pulse compression Matched filter

SOFTWARE IMPLEMENTATION

Vivado

Vivado Design Suite is a software suite developed by Xilinx, a leading company in the field of a programmable logic devices (PLDs). It is designed to facilitate the synthesis and analysis of Hardware Description Language (HDL) designs, offering advanced features for SoC development and high- level synthesis. It provides an integrated design environment (IDE) that encompasses tools for system-level design down to the IC (integrated circuit) level.

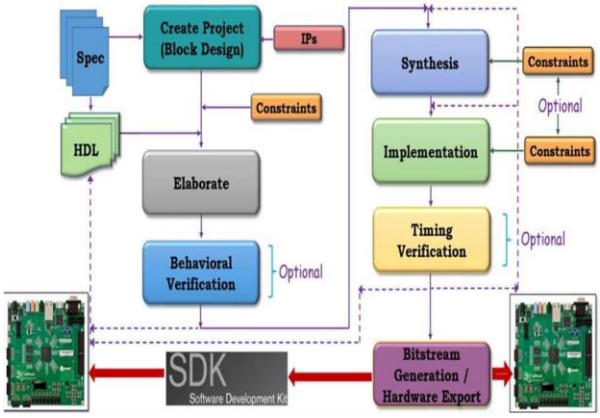


Figure 8 Block Diagram of Vivado flow

MATLAB

MATLAB is a powerful and versatile language specifically designed for technical computing purposes. It offers a comprehensive set of tools and features that make it a popular choice among scientists, engineers, and researchers. With MATLAB, you can perform mathematical calculations, develop algorithms, build models, analyze data, visualize results, create scientific graphics, and even develop applications with graphical user interfaces.

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RESULTS AND DISCUSSIONS

In this paper, we have designed DDC session with40MSps sampling rate, in which NCO generates 10MHz and passes to Mixer. Then mixer output is passed to LPF with the center frequency of 1.5 MHz After filtering it is passed to Decimator whose output is 3MHz with 5MSps. The output ofDDC session is passed to pulse compression session. Results are shown below,

RTL schematic

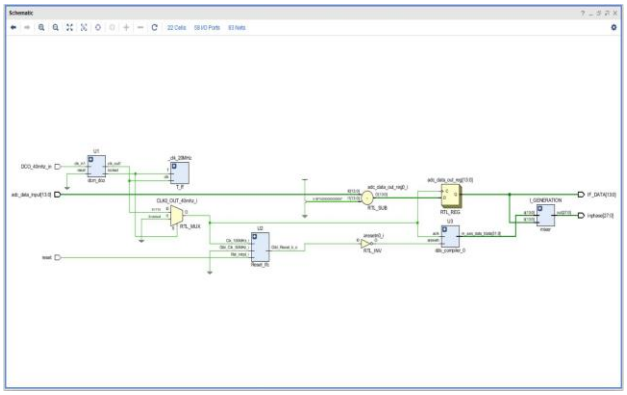

Figure 9 RTL schematic

Simulation results

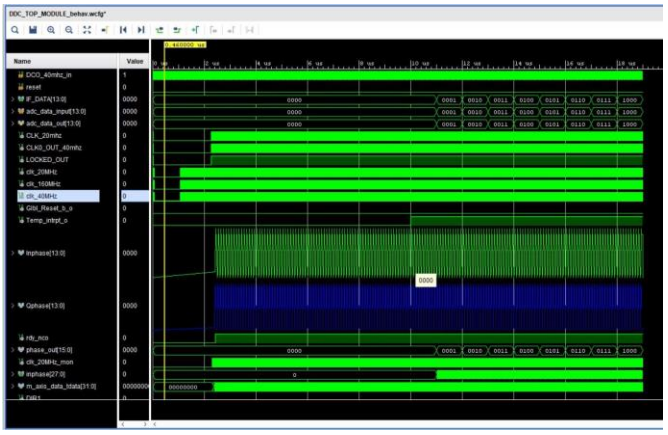

Figure 10 Simulation results

Device Utilization Summary

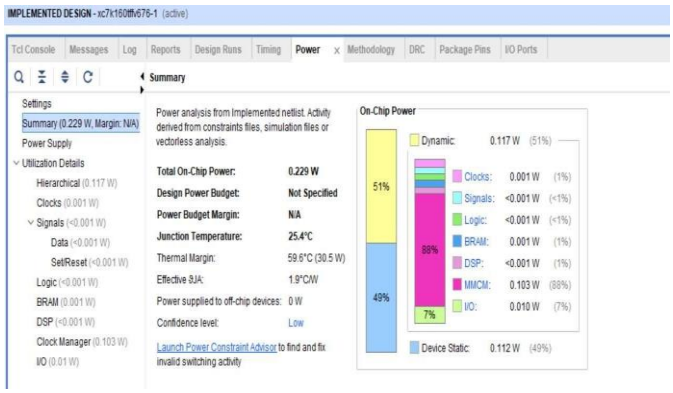

Figure 11 Device Utilization Summary

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MATLAB simulation results:

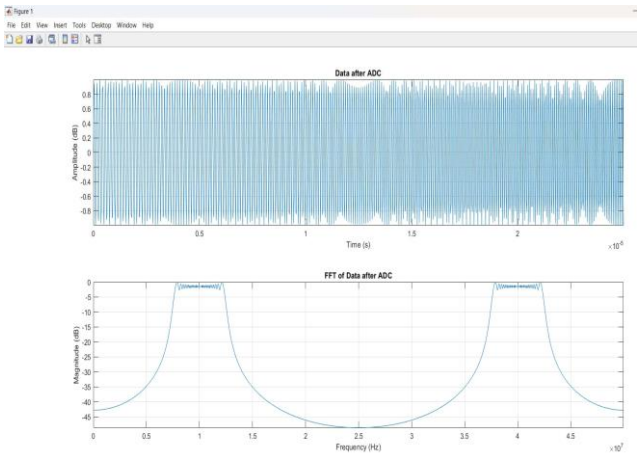

Figure11 Input Signal in Time Domain andFrequency Domain

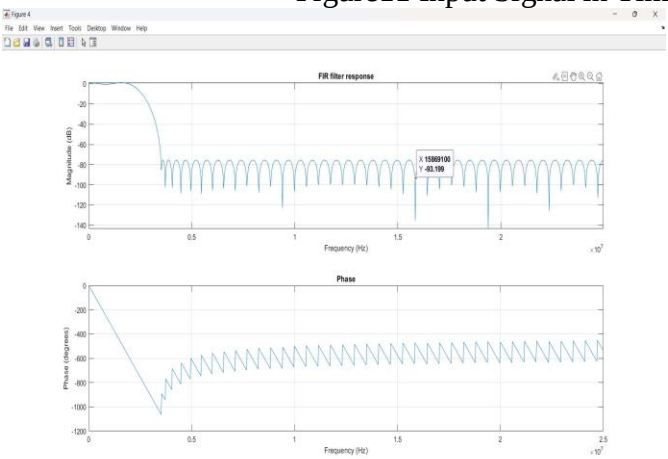

Figure 12 Filter Response of CIC filter

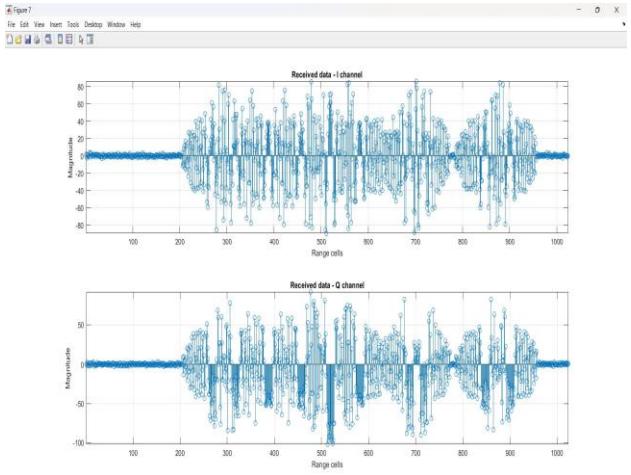

Figure 14 DDC and Pulse compression output

5. Conclusion

An efficient and Flexible real-time pulse compression technique appropriate for digital receiver design was developed. The systemutilizes a very large integrated circuit (VLIC)

architecture to improve performance in radar and communication systems. Key components, such as the digital downconverter (DDC), low-pass filter, and FFT processing and pulse compression were designed and evaluated, showing excellent agreement with theoretical expectations. This allows for easy adaptation of radar working parameters, aligning with SDR stands for software-digital radio. The proposed design is a one-chip solution for both pulse compression and receiver processing.

Further research is recommended for investigating window processing, designing multi- codes within the pulse compression system to overcome ambiguity and exploring novel windows in the frequency domain using FPGA and future work should focus on designing multi-codes within the pulse compression system to avoid confusion.

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